AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0002] with the following amended paragraph:

[0002] Timing circuits are used for a numerous clocking applications, ~~particular~~ particularly in digital communications networks. A typical timing circuit comprises a phase locked loop, particularly a digital phase locked loop in which the output of a digital controlled oscillator, divided by a number n, is fed back to a digital phase detector and compared with the input signal. The output of the phase detector is fed to the input of the digital controlled oscillator through a digital filter.

Please replace paragraph [0003] with the following amended paragraph:

[0003] In typical PLL architectures the output of the PLL is never precisely identical to its input. If the input is steady the output may closely follow the input, but will have a slightly different behavior due to noise. In case the input is not steady, the PLL will try to follow the noise, but necessarily with a relatively late response. In PLL's there is typically no basis on which the future value of the input signal can be predicted. Consequently non-causal filtering is required to accurately track the input signal, which clearly is impossible. If accurate analog delay means were feasible it might be possible to precisely ~~mimiek~~ mimic the delayed input. However, this type of behavior only exists for signal restoration, where the input signal has information, for example, concerning the phase or frequency domain. This may be the case for receivers, where the PLL forms a convoluter that establishes highest accuracy when the signal is most accurately followed.

Please replace paragraph [0006] with the following amended paragraph:

[0006] A conventional radio receiver utilizes no quantization in either time or amplitude in its first stages. The existence of many large disturbances will make amplitude quantization difficult due to the number of required bits; time quantization ~~quantization~~ would lose details on for instance phase information. Instead the use of downconversion and sharp filtering on the generated IF frequency yields the effect of losing undesirable signals. The crucial element in this is that effectively the mixing element (which may be called phase detector) forms a simple convoluter to emphasize the desired signal.

Please replace paragraph [0007] with the following amended paragraph:

[0007] Most phase detectors operate on amplitude discrete, time-continuous basis. The output of the phase detector behaves as an analog signal when looked at over some longer period~~;. with~~ With a low pass filter the phase detector becomes truly analog. This is due to the time continuous inputs of the detector, and this translates into amplitude continuity on the output.

Please replace paragraph [0013] with the following amended paragraph:

[0013] An operation such as switching between two references which are not necessarily in phase ~~MTIE and MTIE reset can relatively well be done~~ performed in analog systems, but requires a measurement/activation cycle, typically ~~with~~using ~~AD and DA~~analog-to-digital and digital-to-analog converters. On switching to the new reference any phase offset is handled so that the output phase appears to remain constant. In Analog solutions the realization of the offset is typically done by subtracting the offset at the output of the phase detector with a digital-to-analog converter. In a digital solution this ~~again~~ operation is much

simpler. ~~(MTIE refers to the switching between two references, which are not necessarily in phase. The MTIE switch means that on the new reference an offset phase is handled so that the output phase seems to remain fixed. In Analog solutions the realization of the offset is typically done by subtracting the offset on the output of the phase detector with a DAC).~~

Please replace paragraph [0014] with the following amended paragraph:

[0014] Flexibility is much greater in the digital domain. Non-linear operations such as changing the low pass frequency are quite straightforward to implement. In the analog domain these operations yield extra demands, which ~~has~~ have a direct impact on accuracies.

Please replace paragraph [0017] with the following amended paragraph:

[0017] In an all digital implementation the error signals will all be in digital format. This makes the use of these values in statistical measurements (average, min, max, mean, deviation etc) relatively trivial. In an analog solution the signals must be converted to digital first, or be handled with very difficult analog ~~ercuits~~circuits. One of the difficult elements in the analog domain is that the signals may have a wildly varying dynamical range from signal to signal, which does not make the implementation simpler.

Please replace paragraph [0020] with the following amended paragraph:

[0020] An all digital PLL has one major drawback~~;~~. ~~the~~ The feedback signal and the reference typically will not be in phase~~,~~ because the ~~object of the~~ PLL ~~to~~ suppresses certain signal artifacts. This lack of phase alignment directly translates to timing errors[[;]]. ~~the~~ The implicit sampling is discrete and therefore has rounding/trunking errors. This in itself may not seem too serious at a first glance, but it has a direct impact on the transfer function of the PLL, which is related to the transfer function of the phase detector.

Please replace paragraph [0032] with the following amended paragraph:

[0032] Figure ~~6shows~~ 6 shows a dual digital phase locked loop in accordance with the principles of the invention;

Please replace paragraph [0055] with the following amended paragraph:

[0055] The first PLL 1 is referred to as an acquisition PLL and has a low pass filter 11 with a relatively high cut-off frequency. For example, 300KHZ, so that the acquisition PLL tracks all changes in the input signal, including error components. The output [[3]] of the first PLL 1 is connected to the input of a second PLL 2, forming an output PLL and generating an output signal [[4]].

Please replace paragraph [0071] with the following amended paragraph:

[0071] Figure 10 shows a plurality of acquisition PLLs 1 connected through operational block 5 to output PLL 1. The acquisition PLLs 1 are connected through Muxes 6 to three inputs in1, in 2, in 3, and crystal oscillator 7. This ~~emodiment~~ embodiment allows ~~allows~~ the quality of the circuits to be tested.

Please replace paragraph [0072] with the following amended paragraph:

[0072] It will be clear that the number of possible and relevant implementations are enormous. The crucial element in this is that once the input is digitized, the operations can be handled error free, just by choosing the correct coding and the appropriate architecture. This opens up a ~~wild~~ wide range of applications, with negligible errors.